Magnetic Technology In Computers To Reduce Power Consumption

Umang, Ramya K M, Avinash P, Komala J

Abstract - In the recent years there is a growing demand of power consumption, which is the measure of prosperity. To fulfil this growing energy demand it is to either increase the generation of energy or reduce the energy losses or consumption in the devices. Recently the trend is switching towards the reduction of energy consumption in the devices and also to reduce the size of the components using modern fabrication technology. One of such is the improvement in fabrication technology of magnets leading to the replacement of electronics circuit in chip by Nano-magnets which helps in reducing the power consumed by the electronic circuits. The work on replacement of the electronic circuits by magnets and designing the computer using array of quantum dots was started an era back but due lack in fabrication technology this seemed a difficult task. Now with the help of improved fabrication technology the idea of making computers by using arrays of quantum dots is possible. The computation time taken is slightly more than electronic circuits though the major advantage of reduced power consumption compensates it.

Index Terms– Quantum Dots, Nano-magnets, Fabrication Technology, Energy Consumption, and Energy Demand.

1 Introduction

When it comes to computing, we can very easily divide the technologies we use into two distinct categories: speedy electronics and stable magnetics. Electrons, which move fast and interact strongly with one another, are ideal for performing computation. Magnets, by contrast, aren't known for their speed, but they're hard to perturb, making them the perfect medium for data storage. But this division may soon disappear. Thanks to modern fabrication technology, we can now create nanometre-scale magnetic devices that can perform computations. These devices are not as speedy as state-of-the-art transistors, but they require far less energy to switch.

There is a need of devices like these because modern chips are consuming too much power. Today, the amount of electricity needed simply to maintain data in a circuit called standby power is fast approaching the amount that's consumed when an actual computation is performed. Magnet based devices, which require no power to save their state, could drastically cut down on this constant power drain, which is one of the main obstacles to continued progress in chips.

One of the most straightforward approaches: building logic gates and wires out of small patches of magnetic material. These "Nano magnets" act just like tiny bar magnets. In circuits made with them, information isn't carried from one place to another electronically. Instead it's transmitted directly poles as it moves from one magnet to the next, in much the same way that a NOT gate reverses the logic state of a bit

Fig. 1. Data acquired in the field of tiny bar magnet.

We have already demonstrated that we can build simple circuits, such as adders, with these Nano magnets. Now, with a new fabrication technique, we're starting to contemplate what can be done to build fully integrated logic chips. Though relatively modest, these achievements make it clear that this technology could someday be used to make ultralow power chips. In some cases we expect that nanomagnet circuits could use a tenth or maybe even a hundredth of the power with no sacrifice in performance. Such capabilities could be ideal for sensors and display electronics, hardware accelerators on multicore chips, and computationally demanding applications such as through the magnetic attractions and repulsions, flipping the magnetic attractions and repulsions, flipping the polarity of north and south

2 Conventional (Electronic) Technology In Computers

- *Department of EEE, East West Institution of Technology, Bengaluru 560091*
E- Mail ID usharma.sharma0@gmail.com

Random-access memory (RAM) is a form of computer data storage. A random-access memory device allows data items to be accessed (read or written) in almost the same amount of time irrespective of the physical location of data inside the memory. Random-access memory (RAM) contains multiplexing and demultiplexing circuitry to connect the data lines to the addressed storage for reading or writing the entry. Usually more than one bit of storage is accessed by the same address, and RAM devices often have multiple data lines and are said to be '8-bit' or '16-bit' etc. devices.

In today's technology, random-access memory takes the form of integrated circuits. RAM is normally associated with volatile types of memory (such as DRAM memory modules), where stored information is lost if power is removed, although many efforts have been made to develop non-volatile RAM chips. Other types of non-volatile memories exist that allow random access for read operations, but either do not allow write operations or have other kinds of limitations on them. These include most types of ROM and a type of flash memorycalled NOR-Flash.

Fig. 2. Example of writable volatile random-access memory: Synchronous Dynamic RAM modules.

The memory cell is the fundamental building block of computer memory. The memory cell is an electronic circuit that stores one bit of binary information and it must be set to store a logic 1 (high voltage level) and reset to store a logic 0 (low voltage machine vision systems in autonomous vehicles process. The value in the memory cell can be accessed by reading it.

The SRAM, static ram memory cell is a type of flip-flop circuit, usually implemented using FETs. These require very low power when not being accessed.

A second type, DRAM is based around a capacitor. Charging and discharging this capacitor can store a '1' or a '0' in the cell. However, this capacitor will slowly leak away, and must be refreshed periodically. Because of this refresh process, DRAM uses more power, but can achieve greater storage densities. However, because of this greater power use, as silicon feature sizes have become smaller, the disadvantages of DRAM's greater power use has outweighed the advantages of smaller size, and very many RAMs sold are now SRAM

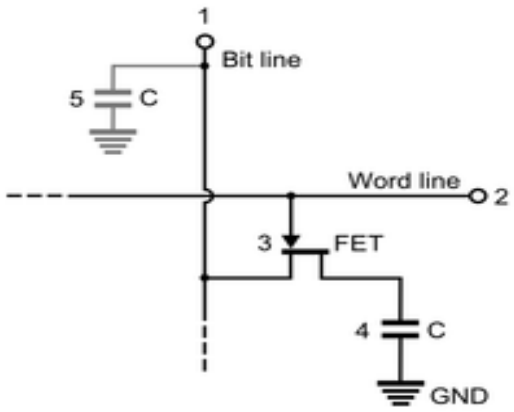


Fig. 3. DRAM Cell (1 Transistor and one capacitor).

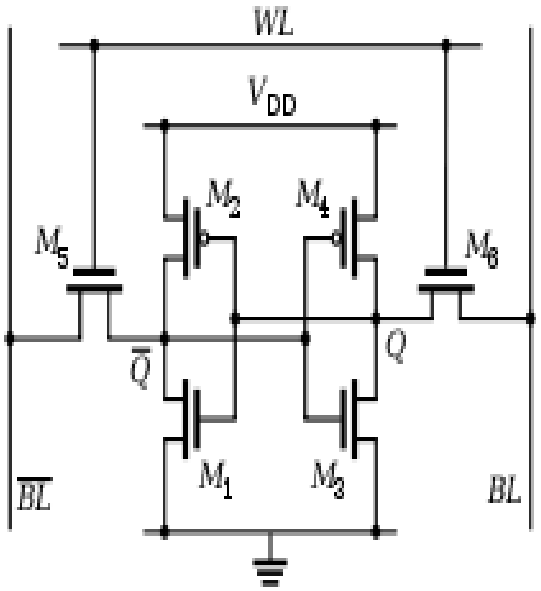


Fig. 4. SRAM Cell (6 Transistors).

3 DESIGN OF MAGNETIC CHIP

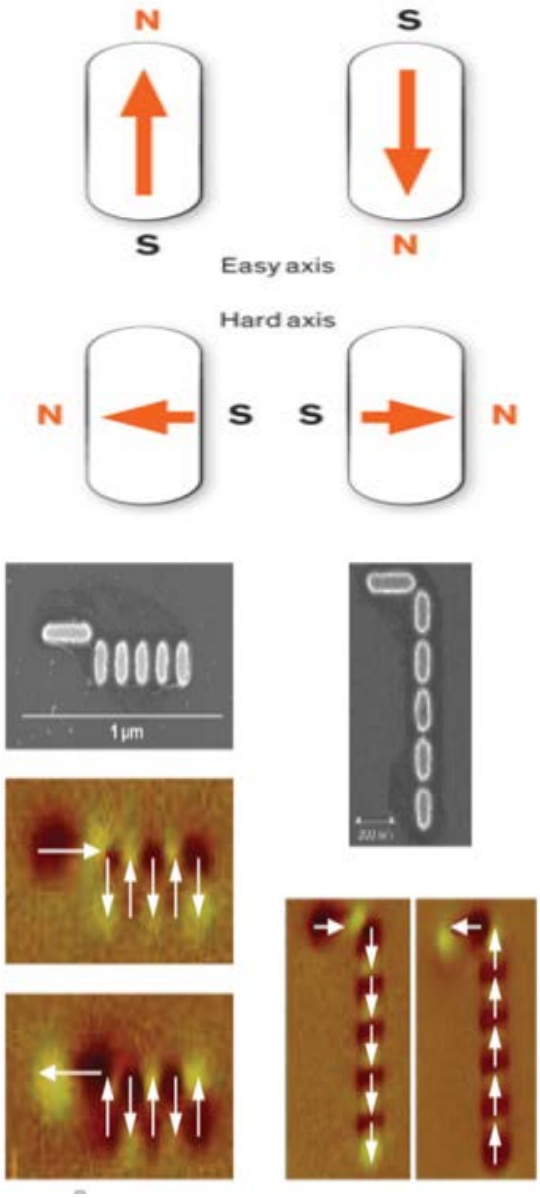


Fig. 4. The magnetic field of an elliptical nanomagnet naturally prefers to align along the longer, or "easy," axis [top illustrations]. Wires can be constructed in two ways. One is by arranging the magnets side by side [centre], where their magnetizations prefer to alternate in direction. The other is end to end [right, down], where all magnetizations prefer to point in the same direction. All arrows point north

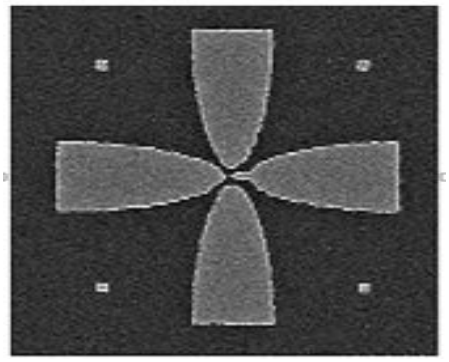
Take a magnet smaller than the material's domain size—typically around 100 nanometres across—and to make a tiny version of a permanent magnet. As with a bar magnet or a compass needle, the magnetic field of a nano magnet naturally prefers to align itself on the longer axis with a north pole on one end and a south pole on the other. But by fine tuning the aspect ratio—the ratio of height to width—we can make it so that it requires relatively little energy to flip the direction of the nano magnet's north and south poles. In fact, if you make a nanomagnet too round—or too small, for that matter—little kicks from the thermal energy in the material can cause that flip to happen on its own at random. Today we use similar tiny, flippable nanomagnets to store information in ordinary hard disk drives. They can also be found in magnetic RAM technologies now under development. In both of these cases, we don't want the magnetic bits to interact with one another, such interactions would risk corrupting the data that you're trying to store. But when building nanomagnetic logic, those interactions are exactly what you need in order to connect the devices and make them perform computations.

The idea was to try to make computers by using arrays of these dots, which are patches of semiconductor in which electrons are confined to a space so small that they exhibit the same quantum behaviour that they would in an atom. Rather than using wires, neighbouring dots would transmit information by the Coulomb forces, which attract opposite charges and repel like charges.

4 Properties Of Nano-Magnets

They're inherently insensitive to radiation, they can switch pretty much indefinitely without degradation, and they're non-volatile, requiring no energy to retain data when they're not switching.

At the same time, they're very slow by modern transistor standards, maxing out at about one hundredth the speed of a traditional transistor. That means nanomagnet logic will likely never reach gigahertz speeds. But the potential energy savings still make it an attractive alternative for the many applications that don't require such speeds.



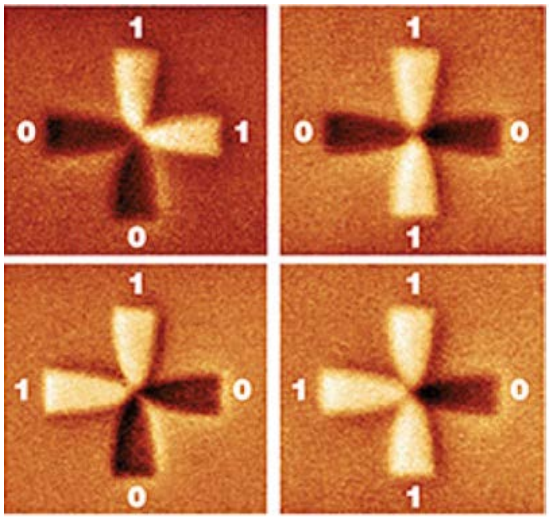


Fig. 5. Four or five nanomagnets can be arranged to form a key circuit component: the majority logic gate. This gate outputs the state that the majority of the inputs are in—or in this case, the inverse of that state. Three 1s, for example, will yield a 0. Note that this gate is built from nanomagnets with an out of plane magnetization—more on this design in the final section of the article

5 Moving Information In Magnetic Circuits

Much of the energy advantage comes in at the circuit level. Because of the way nanomagnets interact to perform logic operations, it can take as few as five magnets to add two 1bit numbers together. For comparison, it can take 20 to 30 transistors to construct a similar adder in silicon.

But even early on, we realized that any nanomagnet computer we build will be only as good as its clock. As we mentioned before, we need clocking circuitry to keep computations moving in the right direction. We also need a clock to get the nanomagnets to switch reliably. Because magnets are so stable—the very reason they're commonly used for data storage—switching them is often the tricky part. On its own, the fringing field surrounding one dot isn't strong enough to reliably induce a 180degree switch in a neighbouring magnet. A clock signal can help a nanomagnet switch. It could be created with something as simple as a nearby wire, which would generate an extra magnetic field near a nanomagnet when it's carrying a current. To see how such a clock would work, imagine an elliptical nanomagnet. As noted before, its natural state is to have its magnetization along its longer axis. If we use the added wire to apply an additional magnetic field, called a switching field, we can rotate the nanomagnet's magnetization by

90 degrees into what's called the "hard" axis, the shorter axis of the two. This is an unstable state for the nanomagnet, and when the switching field is removed, the magnetization will begin to snap back into either one of two directions along its longer, "easy" axis.

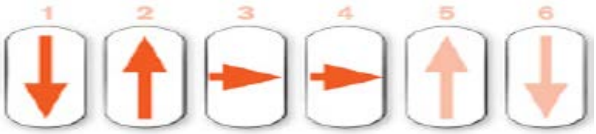
When it starts to do so, the fringing fields from the neighbouring magnets will determine which direction it falls into.

To start a chain of spin flips, first use a strong magnetic field to flip magnet 1.

Magnet 2, originally in a down configuration, must flip up to propagate the information to the right. The magnetic field of magnet 1 Isn't strong enough to do this on its own. So, the magnetic field from a wire, or clock, is first used to draw magnet 2's magnetism into the metastable "hard" axis

Magnet 2 can now relax into a new stable state. But it's not clear which way it will fall; the field from magnet 1 would have it point up, and the field from magnet 3 would have it return to a down state. To make sure that magnet 2 feels a stronger influence from magnet 1, magnet 3 can be clocked as well.

When the clock signal is now removed from magnet 2, it will relax into an up state, advancing information to the right. Magnet 4 can now be clocked to keep the flow of information going.



Controlling every nanomagnet would require clocking circuitry for each device. In practice, a line of nanomagnets might be clocked in groups. A wire, for example, might control half a dozen nanomagnets at once. The result will be a little more error prone but easier to manufacture

6 STORING THE INFORMATION IN MAGNETIC CIRCUITS

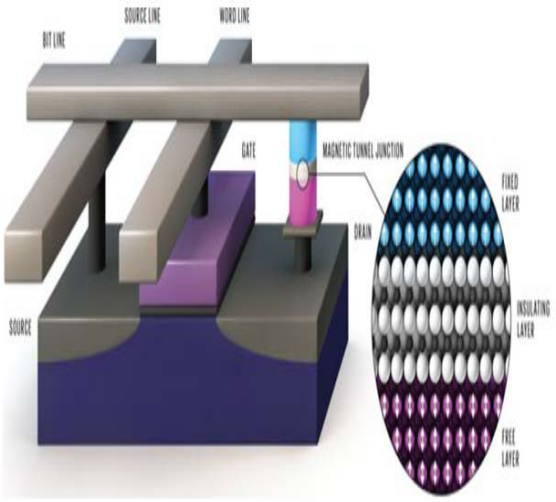


Fig. 7.Storing the information in the magnetic memory

Both spin transfer torque MRAM (STTMRAM) and magneto electric RAM (MERAM) can use the same basic architecture to store data in the orientation of electron spin. Each bit in an array can be accessed at the intersection of two lines of electrodes—a source line and a bit line. A third electrode—the word line—is used to control voltage supplied to the bit. A single bit of information can be stored in the free layer of each magnetic tunnel junction. In STTMRAM, current flows directly through the junction in order to write the bit. MERAM, which boasts a thicker insulating layer, does not permit current to flow as readily and instead uses voltage associated effects to change the state of the bit. In each case, the magnetization of the free layer can be flipped [inset, right]. When the magnetization of the free layer and that of the fixed layer (which serves as a reference) point in the same direction, resistance is relatively low. It is higher when the two magnetizations point in opposite directions. Note that a MERAM transistor is much smaller than an STT MRAM transistor, since it does not have to provide as large a current. As a result MERAM cells are smaller overall, and arrays of them can be made denser

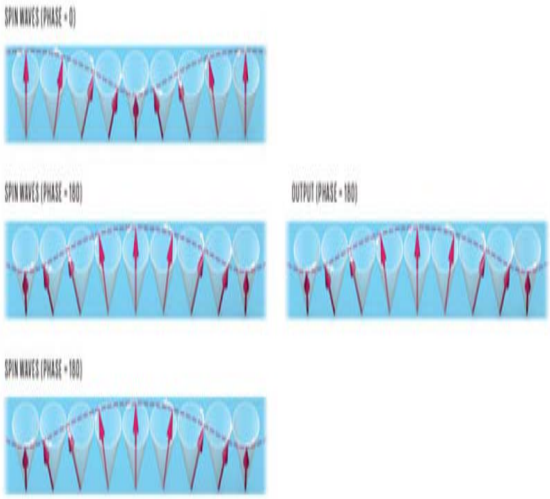


Fig. 6. Moving information in magnetic circuits

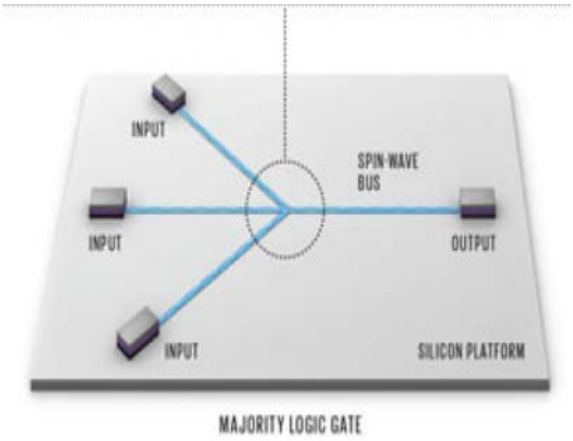


Fig. 8.Riding the waves.

IMPLEMENTATION OF FULL

A voltage pulse can be used to knock an electron's spin out of alignment, causing it to precess. This effect can be used to transmit information along a strip of magnetic material. The first perturbed spin will affect its neighbour and cause a wave of precessing spins to propagate down the line of electrons [top]. These waves can be made to take on two different phases, separated by 180 degrees, to represent a binary 0 and 1. Two waves with opposite phases can be made to interfere with one another, cancelling out the spin perturbation. Logic gates, such as the majority gate, can take advantage of this interaction. The majority gate "votes" for whatever state constitutes the majority of inputs. This can be accomplished as shown [right], by causing three lines of spin-wave inputs to meet and interact. It can also be implemented along a single line, by introducing the voltage pulses that trigger spin-wave perturbations at three different points. In either case, MERAM memory cells can be built on top of the logic gate to

6 Adder Circuit

Up to three horizontal magnets provided the input to a single computing dot and the information was passed along short magnetic wires. The basic, most simple design of the full adder would include AND or OR gates. The fundamental building block of NML is the majority gate, from which it is straightforward to realize the full adder directly. Such a design of the full adder was proposed in, proving the operation using five three-input majority gates (Fig. 9a). A smaller design was introduced in where the circuit is composed of only three three-input majority gates (Fig. 9b).

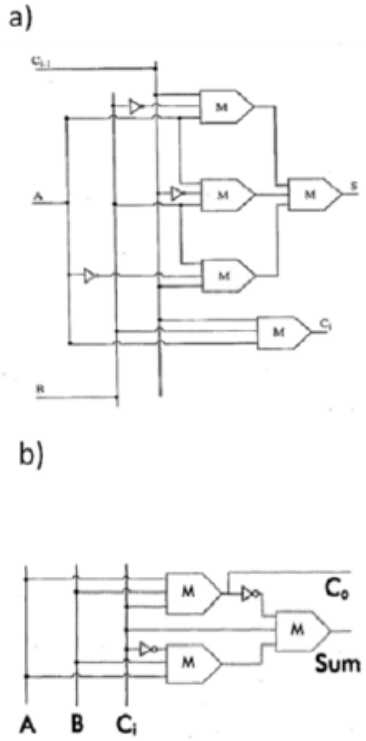


Fig. 9.a) An early full adder design from to be built from two-state building blocks. b) The smallest full adder design proposed in several publications (only 3 majority voting gate is necessary for the implementation).

retain input data, trigger spin waves, and read out the result.

TRUTH TABLE FOR FULL ADDER CIRCUIT

Table. 1.Truth table of full adder circuit

A	B	Carry-In	Sum	Carry-Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

.

Fig. 10. Shows a possible nanomagnetic layout with three three-input majority gates (cross point of the horizontal and the vertical nanomagnet wires) built in.

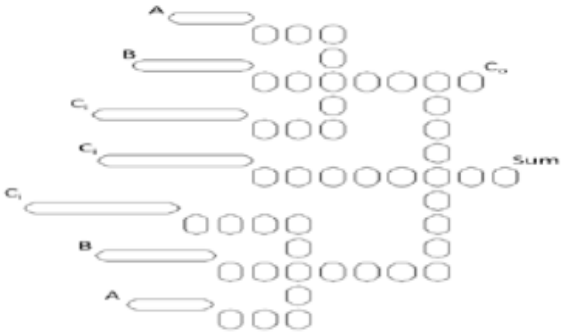


Fig. 10.Schematic of the full adder includes three three-input majority gates, and several high aspect ratio magnets to act as drivers providing the input data for the circuits.

7 Conclusion

The long magnets in the left side of the circuit in Fig.2 are the programmable drivers providing the data for testing the adder. A particular Bext applied field can switch only magnets with a switching field (coercivity) Bsw < Bext. Higher aspect ratios yield to higher switching fields. Therefore, a globally applied magnetic field can switch only magnets smaller than a certain length.. The thicknesses of the dots are 20 and 30 nm, their width is fixed at 60nm, and the coercivity is plotted as the function of their length. The field is applied at a 45° angle to the long axis of the magnets. Exploiting aspect ratio as a design variable, the driver magnets can be set separately, resulting in a programmable circuit.

Magnetic circuit consumes 10 times less power than conventional (electronic) circuit. It is hard to perturb the data. It is compact in design. It is cheaper than conventional circuits to design. But the data transfer speed is slower compared to electronic circuits.

REFRENCES

[1] Varga, G. Csaba, G. H. Bernstein, and W. Porod," Implementation of a Nanomagnetic Full Adder Circuit", University of Notre Dame, Notre Dame, IN, 46556, USA,2011.

[2] Wolfgang Porod& Michael Niemier, "Building Ultra-Energy-Efficient Computers Out of Tiny Bar Magnets", University of Notre Dame, in Indiana,2015.

[3] Markus Becherer, Gy¨orgyCsaba, Wolfgang Porod, Fellow, IEEE, Rainer Emling, Paolo Lugli and Doris Schmitt-Landsiedel, "Magnetic Ordering of Focused-Ion-Beam Structured Cobalt-Platinum Dots for Field-Coupled Computing",2008.